REMARKS

The Office Action mailed on May 3, 2006 has been reviewed. Claims 1, 2, 4, 5, 7-10, 12, 13, 18-17, 19-22, 24-26, 28 and 30-34 are pending in this application.

Claim Objections

Claim 1 was objected to for citing an "expected quality level". The Office Action took the position that, "after further review of the specification, it seems the applicant is comparing the quality level of the reference clock signal with the quality level of the phase locked loop, which is constantly changing. Since the quality level of the phase locked loop is constantly changing, it cannot be considered expected." This is an incorrect characterization of the claim language. The claim language, in relevant part states, "when a quality level of the reference clock signal indicated by the status message is less than an expected quality level of the phase locked loop in the holdover condition." The comparison is between "a quality level of the reference clock signal indicated by the status message" and "an expected quality level of the phase locked loop in the holdover condition" (that is, the expected quality level of the PLL if it were placed in the holdover condition).

Accordingly it is respectfully requested that this claim objection be withdrawn.

Claims 28 and 34 were objected to being substantial duplicates of claims 26 and 33, respectively.

Claim 26 recites, in part, "during a time when the primary reference clock signal is failed or *has an indicated quality level below the target level*, and when a secondary reference clock signal is valid and has an indicated quality level at or above the target level: . . ." while claim 28 recites, in part, "during a time when the primary reference clock signal either is failed or *is valid and has an indicated quality level below the target level*, and when a secondary reference clock signal is valid and has an indicated quality level at or above the target level: . . .". That is, claim 26 recites a particular condition "when the primary reference clock signal . . . has an indicated quality level below the target level" (that is, regardless of the validity of the primary reference

clock signal) versus claim 28, which recites "when the primary reference clock signal . . . is valid and has an indicated quality level below the target level" (conditioned on validity of the primary reference clock signal in addition to its quality level). The Office Action contains no explanation as to why such a difference is insubstantial. Therefore, it is respectfully submitted that claims 26 and 28 are not substantial duplicates of one another.

It is respectfully submitted that similar arguments apply to claims 33 and 34.

Accordingly, it is respectfully requested that these claim objections be withdrawn.

Rejections Under 35 U.S.C. § 103

Claims 1, 2, 4, 5, and 7-9 were rejected under 35 USC § 103(a) as being unpatentable over Zhang et al. (U.S. Patent No. 6,304,582) in view of Zampetti et al. (U.S. Patent No. 6,943,609). Applicant traverses this rejection and requests reconsideration.

Claim 1 of the present application recites, in part, "wherein the instructions stored on the machine-readable medium are capable of causing the processor to place the phase locked loop in the holdover condition when a quality level of the reference clock signal indicated by the status message is less than an expected quality level of the phase locked loop in the holdover condition."

The Office Action cited "Fig. 8, label aging conditions and meet conditions to update DAC_in_aging?, Col. 19, lines 9-34 and Col. 14, lines 14-40" to support its contention that Zhang teaches "an expected quality level of the phase locked loop in the holdover condition" as recited in claim 1 of the present application. That is, the Office Action is citing the "aging processing steps" of FIG. 8. However, ignoring for the moment whether the results of the aging processing steps of FIG. 8 can properly be considered "an expected quality level of the phase locked loop in the holdover condition" (which Applicant does not concede), the results of the aging processing steps of FIG. 8 are not used to determine when to place the phase locked loop into the holdover condition; instead, Zhang clearly indicates that such results are used for processing the occurs when the PLL is in holdover condition but not to determine if and when to

enter holdover. See, e.g., Zhang, FIG. 9 (please note the decision block labeled "Meet conditions to get out of Holdover?") and Col. 19, lines 7-24 which state:

> In holdover state, Sync Controller selects an open loop mode of operation (as there is no reliable reference clock to lock to).
>
> The holdover operation procedure is illustrated in FIG. 9. As shown in FIG. 8, a forward linear prediction process is applied to the recorded DAC_in_aging sequence in order to determine an estimation of the value of DAC_in_holdover in the event of a holdover.
>
> This predicted value is retrieved when the system first selects the Holdover (open loop) mode of operation during the initial Prediction Processing for DAC_in_holdover step. Then, for each subsequent iteration, the predicted DAC_in_holdover value is adjusted based on measurable conditions, for example the measured temperature. These adjustments are made at the same rate as the highest state operation rate of the multistate filters.
>
> These steps continue until the conditions for Sync module to return to its original state from holdover state (called Holdover_out) are satisfied. These conditions are based on determining the quality of any received T1 reference signal has improved until the above described fault detection conditions are no longer satisfied. . . .

Zhang, Col. 19, lines 7-24 (emphasis added). Instead, Zhang teaches two reasons to go into holdover, a lost reference or a bad reference. According to Zhang, the bad reference threshold is "defined according to a frequency offset which is known to exceed the normal operating bounds of the T1 reference source. Preferably the sync system with [sic] send an indication to the network element which produces the T1 reference signal of the bad reference condition detected." Col. 14, lines 35-40. This simply does not teach or suggest "wherein the instructions stored on the machine-readable medium are capable of causing the processor to place the phase locked loop in the holdover condition when a quality level of the reference clock signal indicated by the status message is less than an expected quality level of the phase locked loop in the holdover condition" as recited in claim 1 of the present application.

Moreover, the Office Action took the position that the slip information 235 is "a status message indicative of a quality level of the reference clock signal" as recited in claim 1 of the present application. However, assuming for the sake of argument that this is correct (which Applicant does not necessarily concede), nowhere does Zhang teach or suggest using such slip information in determining when to place a phase locked loop into a holdover condition.

Claims 2, 4, 5, and 7-9 were rejected in part using the same reasoning as was used to reject claim 1. Accordingly, it is respectfully submitted that at least the arguments set forth above with respect to claim 1 apply to these claims as well.

Based on the foregoing, it is respectfully requested that this rejection be withdrawn.

Claims 10, 12-13, and 15 were rejected under 35 USC § 103(a) as being unpatentable over Zhang et al. (U.S. Patent No. 6,304,582) in view of Zampetti et al. (U.S. Patent No. 6,943,609) and further in view of Dubberley et al. (U.S. Patent No. 5,581,555). Applicant traverses this rejection and requests reconsideration.

Apparently, the Office Action rejected these claims based in part on the same reasoning as claim 1. Therefore, it is respectfully submitted that at least the arguments set forth above with respect to claim 1 apply to these claims as well. Based on the foregoing, it is respectfully requested that this rejection be withdrawn.

Claim 16 was rejected under 35 USC § 103(a) as being unpatentable over Zhang et al. (U.S. Patent No. 6,304,582) in view of Zampetti et al. (U.S. Patent No. 6,943,609) and further in view of Dubberley et al. (U.S. Patent No. 5,581,555) and further in view of Baydar et al. (U.S. Patent Publication No. 2002/0097743). Applicant traverses this rejection and requests reconsideration.

Apparently, the Office Action rejected these claims based in part on the same reasoning as claim 1. Therefore, it is respectfully submitted that at least the arguments set forth above with

respect to claim 1 apply to these claims as well. Based on the foregoing, it is respectfully requested that this rejection be withdrawn.

Rejections Under 35 U.S.C. § 102

Claims 17 and 19 were rejected under 35 USC § 102(e) as being anticipated by Zhang et al. (U.S. Patent No. 6,304,582).

Claim 17 has been amended to incorporate the language previously recited in claim 19. Claim 19 has been cancelled. It is respectfully submitted that at least the arguments set forth above with respect to claim 1 apply to claim 17 as well. Based on the foregoing, it is respectfully requested that this rejection be withdrawn.

Rejections Under 35 U.S.C. § 103

Claims 20-22, and 24 were rejected under 35 USC § 103(a) as being unpatentable over Zhang et al. (U.S. Patent No. 6,304,582) in view of Zampetti et al. (U.S. Patent No. 6,943,609).

It is respectfully submitted that at least the arguments set forth above with respect to claim 1 apply to claims 20-21 as well.

Claim 22 recites in part "placing the phase locked loop in a holdover condition if the quality level indicated by each status message is below a target level regardless of a validity of any reference clock signal". As noted above in connection with claim 1, even assuming for the sake of argument that the slip information 235 can properly be considered a status message as recited in claim 22, nowhere does Zhang teach or suggest using such slip information in determining when to place a phase locked loop into a holdover condition.

Claim 24 depends from claim 22; therefore, at least the arguments set forth above with respect to claim 22 apply to claim 24 as well.

Based on the foregoing, it is respectfully requested that this rejection be withdrawn.

Claims 25-26, and 30-34 were rejected under 35 USC § 103(a) as being unpatentable over Zhang et al. (U.S. Patent No. 6,304,582) in view of Zampetti et al. (U.S. Patent No. 6,943,609).

Claim 25 ultimately depends from claim 22; therefore, at least the arguments set forth above with respect to claim 22 apply to claim 25 as well.

With respect to claim 26, Applicant is having a difficult time understanding the rejection set forth in the Office Action. It is respectfully submitted that the Office Action fails to set forth a prima facie case of obviousness since the Office Action fails to explain how each and every limitation set forth in the claim is taught or suggestion by the proposed combination. For example, the Office Action has failed to explain how the following language of claim 26 has been taught or suggested by the proposed combination:

> during a time when the primary reference clock signal is failed or has an indicated quality level below the target level, and when a secondary reference clock signal is valid and has an indicated quality level at or above the target level:
>
> generating a second error signal indicative of a phase relationship between the secondary reference clock signal and a second feedback signal;
>
> filtering the second error signal to produce a second control signal;
>
> generating the timing signal in response to the second control signal; and
>
> deriving the second feedback signal from the timing signal; and

Moreover, it appears that the Office Action fails to explain how the cited references would be combined and fails to provide any motivation for combining the cited references.

Claims 28 and 30-34 were rejected based on reasoning used to reject other claims, such reasoning already having been addressed by Applicant herein.

Based on the foregoing, it is respectfully requested that this rejection be withdrawn.

CONCLUSION

Applicant respectfully submits that claims 1, 2, 4, 5, 7-10, 12, 13, 18-17, 19-22, 24-26, 28 and 30-34 are in condition for allowance and notification to that effect is earnestly requested. If necessary, please charge any additional fees or credit overpayments to Deposit Account No. 502432.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at 612.455.1681.

Respectfully submitted,

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